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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
Analog.7020	

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Patent and Trademark Office, via EFS-Web on the date shown below.

on 11-13-06

Signature Elizabeth M Ball

Typed or printed name Elizabeth M. Ball

Application Number	Filed
10/715,629	11/17/2003
First Named Inventor	
Frederic Boutaud	
Art Unit	**Examiner**
2181	Vincent Lai

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 33,298
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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11/13/06
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Arguments to be Considered by Pre-Appeal Brief Conference Panel

I. Rejection under 35 U.S.C. §102(b)

Claims 1-14 have been rejected under 35 U.S.C. §102(b) as being anticipated by Morley (US-A-4,276,594). This rejection under 35 U.S.C. §102(b) is respectfully traversed.

A. Independent Claim 1

The Examiner alleges that Morley discloses determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle. The Examiner points to column 58, lines 17-20, of Morley to support this allegation. Column 58, lines 17-20, states, "The 6800 accesses this RAM during the PHΦ of the MIO cycle. During serial I/O, this time is used to fetch/store characters and update pointers. For parallel I/O, this is used to fetch parameters for the PIA."

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any determination with respect to the number of unified memory accesses that would be required during a single instruction cycle. At column 58, lines 17-20, Morley teaches that the RAM includes a parallel I/O port and a serial I/O port. Moreover, Morley teaches that the RAM is access through the Serial I/O and the Parallel I/O to fetch data from the memory. Notwithstanding the use of both the Serial I/O and the Parallel I/O to fetch data from the memory, Morley fails to teach determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle for proper execution of the fetched program instruction since only two fetches are discussed.

In response to this argument, the Examiner states that it is the Examiner's interpretation of the teachings of Morley that "the number of unified access [sic] **can be** determined and three unified accesses **is** [sic] **possible**." [Emphasis added.] The Examiner further states, "the system [of Morley] has the capability to perform a determination **if** a request for a determination is made." [Emphasis added.] Notwithstanding these assertions, the Examiner has failed to identify any passages in Morley to support the Examiner's allegations.

In other words, absent any specific passages of in Morley that teach making a request to determine the number of unified memory accesses that would be required during a single instruction cycle and follow-up determination, the Examiner's assertions are mere conjecture of what Morley could possibly teach as the Examiner has failed to provide any specific evidence to the contrary.

The Examiner also alleges that Morley discloses accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access and points to column 58, lines 17-20, of Morley to support the allegation. Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose any type of dummy access of the unified memory. Thus, this passage of Morley cannot provide any basis for a finding of anticipation to the limitation corresponding to accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access of independent claim 1.

Lastly, the Examiner alleges that Morley discloses accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access and points to Figure 28 to support the allegation. With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and placed on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access, as set forth by independent claim 1.

In summary, with respect to independent claim 1, Morley fails to teach (1) determining if the fetched program instruction would require three unified memory accesses during a single instruction cycle for proper execution of the fetched program instruction; (2) accessing the unified memory a first time, during the instruction cycle associated with the fetched program instruction, with a dummy access; and/or (3) accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access.

B. Independent Claim 6

The Examiner alleges that Morley discloses accessing the unified memory a first time during the second instruction cycle with a dummy access when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity and points to column 58, lines 17-20, of Morley to support the allegation.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose accessing the unified memory a first time during the second instruction cycle with a dummy access when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity, as set forth by independent claim 6. Column 58,

lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory a first time during the second instruction cycle with a dummy access when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity, as set forth by independent claim 6.

Also, the Examiner alleges that Morley discloses accessing the unified memory a second time during the second instruction cycle to read a new instruction when it is determined the program instruction accessed for a second instruction cycle is a conditional program code discontinuity, thereby delaying the instruction access from the unified memory for the second instruction cycle by a half cycle and points to Figure 28 to support the allegation. With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access, as set forth by independent claim 6.

In summary, with respect to independent claim 6, Morley fails to teach (1) accessing the unified memory a first time during the second instruction cycle with a dummy access when it is determined that the program instruction accessed for a second instruction cycle is a conditional program code discontinuity; and/or (2) accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access.

C. Independent Claim 9

The Examiner alleges that Morley discloses accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access and points to column 58, lines 17-20, of Morley to support the allegation.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access, as set forth by independent claim 9. Column 58, lines 17-20, of Morley merely teaches that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access, as set forth by independent claim 9.

Moreover, the Examiner alleges that Morley discloses accessing the unified memory a second time, during the instruction cycle associated with the fetched last instruction of loop, with a data access and points to Figure 28 to support the allegation. With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access, as set forth by independent claim 9.

In summary, with respect to independent claim 9, Morley fails to teach (1) accessing the unified memory a first time, during the instruction cycle associated with the fetched last instruction of loop, with a dummy access; and/or (2) accessing the unified memory a second time, during the instruction cycle associated with the fetched program instruction, with a data access.

D. Independent Claim 13

The Examiner alleges that Morley discloses accessing the unified memory with a dummy access during execution of the last instruction of the loop and points to column 58, lines 17-20, of Morley to support the allegation.

Contrary to the Examiner' position, this passage of Morley fails to discuss or disclose accessing the unified memory with a dummy access during execution of the last instruction of the loop as set forth by independent claim 13. Column 58, lines 17-20, of Morley merely teaches

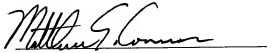
that the RAM may include a parallel I/O port. Column 58, lines 17-20, of Morley is void of any teachings directed to accessing the unified memory with a dummy access during execution of the last instruction of the loop, as set forth by independent claim 13.

Moreover, the Examiner alleges that Morley discloses accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop and points to Figure 28 to support the allegation. With respect to Figure 28, the read operation illustrates that during the PHΦ of the MIO cycle, the data from the memory is accessed and place on the bus; during the PH1 of the MIO cycle, the data sits on the bus; and during the PH2 of the MIO cycle, the data on the bus is uploaded or read. Thus, the memory is only access once per MIO cycle and fails to anticipate accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop, as set forth by independent claim 13.

In summary, with respect to independent claim 13, Morley fails to teach (1) accessing the unified memory with a dummy access during execution of the last instruction of the loop; and/or (2) accessing the unified memory, a second time, with a data access during execution of the last instruction of the loop.

Accordingly, in view of all the reasons set forth above, the Pre-Appeal Brief Conference Panel is respectfully requested to reconsider and instruct the Examiner to withdraw the present rejection under 35 U.S.C. §103.

Respectfully submitted,



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